WHAT IS CLAIMED IS:

1. A Content Addressable Memory ("CAM") architecture providing improved speed, comprising:

- an array of CAM cells connected to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and/or writing data in the array of CAM cells respectively,
- outputs of the said CAM cell are coupled to a match block providing match outputs signal lines that identifies a match/no-match at the end of a search operation, and;
- a control logic for implementing search and address decoding operations during first state and enabling read-or-write operations within the second state of the same clock cycle in the event of a match.

2. The CAM architecture as claimed in claim 1, wherein the control logic comprising a sequencing circuit that enables the data comparators of the CAM cell array and the address decoder of read/write block during the first state of the clock and enables the read-or-write operation in the second state of the same clock.

3. A method for improving speed of a Content Addressable Memory ("CAM") architecture in steps of:

- connecting an array of CAM cells to a compare-data-write-driver and to a read/write block, for receiving the compare-data and for reading and writing data in the CAM cell respectively,
- coupling a match block to said array of CAM cell providing match outputs signal lines for identifying a match/no-match at the end of a Search operation,
- performing the search and address decoding operations during first state of the clock cycle, and;
- implementing the read/write operation after a successful search during the second state of the same clock cycle.